[0031] FIG. 26 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 1.

[0032] FIG. 27 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 1.

[0033] FIG. 28 is a schematic view of the process step of Fig. 5 applied to the embodiment of Fig. 2.

[0034] FIG. 29 is a schematic view of the process step of Fig. 6 applied to the embodiment of Fig. 2.

[0035] FIG. 30 is a schematic view of the process step of Fig. 6 applied a second time to the embodiment of Fig. 2.

[0036] FIG. 31 is a schematic view of the two process steps of Fig. 7 applied to the embodiment of Fig. 2.

[0037] FIG. 32 is a schematic view of the two process steps of Fig. 8 applied to the embodiment of Fig. 2.

[0038] FIG. 33 is a schematic view of the two process steps of Fig. 9 applied to the embodiment of Fig. 2.

[0039] FIG. 34 is a schematic view of a semiconductor device having two sets of symmetric ion implants.

[0040] FIG. 35 is a graph of device performance compared with performance of a device having symmetric halo implants.

[0041] FIG. 36 is a graph indicating SCE or punch through effect on device performance as a function of gate length.

## DETAILED DESCRIPTION

[0042] With reference to Fig. 1, an embodiment of the present invention, which is indicated as Dd, resides in a semiconductor device 1 comprising: a source 2 , an oxide-supported gate 3, supported on a film of oxide 3a, and a drain 4, all of which are supported lengthwise on a semiconducting substrate 5.

[0043] The source 2 includes a shallow source extension 2a and a deep source portion 2b in a source-drain region. The drain 4 includes a shallow drain extension 4a